REMARKS

The specification is amended to correct clerical errors. No new matter is introduced by the amendments to the specification.

Claims 1, 2 and 4 are pending in the present application. Claims 1 and 4 are amended above. Claim 2 is canceled above. No new matter is added by the claim amendments or new claim.

Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Takeuchi, *et al.* (U.S. Patent Number 6,297,797 - hereinafter "Takeuchi). In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over Takeuchi. Accordingly, reconsideration of the rejections is requested.

In accordance with the applicants' invention, an MPEG decoder includes an OSD controller that transforms OSD object data into a pixel data output in response to an enable signal and outputs the pixel data as pixel data output. The OSD controller comprises an OSD buffer that stores the OSD object data received from the CPU and an OSD processor. The OSD processor comprises a buffer interface unit, a text OSD module, a bitmap OSD module, and an OSD mixer. The buffer interface unit receives the OSD object data from the OSD buffer and outputs the OSD object data. The text OSD module receives the OSD object data as text OSD data and transforms the text OSD data and outputs text pixel data. The bitmap OSD module receives the OSD object data as bitmap OSD data and transforms the bitmap OSD data and outputs bitmap pixel data. The OSD mixer receives the text pixel data and the bitmap pixel data, and outputs a resulting mixture of the text pixel data and the bitmap pixel data as the pixel data output.

The features set forth in the amended claims are illustrated at least at Figures 2-3 and

pages 5-6 of the present specification. In this example, an OSD controller 280 includes an OSD buffer 282 and an OSD processor 284. The OSD buffer 282 stores the OSD object data OSD_OBJ received from the CPU 270. The OSD processor 284 reads the OSD object data OSD_OBJ from the OSD buffer 282, and transforms the OSD object data OSD_OBJ into pixel data OSD_OUT. The OSD processor 284 comprises a buffer interface unit 32, a text OSD module 34, a bitmap OSD module 36, and an OSD mixer 37 (see Figure 3 of the present specification). The text OSD module 34 receives from the buffer interface unit 32 the OSD object data OSD_OBJ as text OSD data. The bitmap OSD module 36 receives from the buffer interface unit 32 the OSD object data as bitmap OSD data. The text OSD module 34 transforms the received text OSD data as text pixel data and outputs the transformed text pixel data, and the bitmap OSD module 36 transforms the received bitmap OSD data as bitmap pixel data and outputs the transformed bitmap pixel data. The OSD mixer 37 receives the text pixel data and the bitmap pixel data, mixes them, and outputs the result of the mixture of the received text pixel data and the bitmap pixel data as the pixel data output OSD_OUT. The video mixer 250 mixes the pixel data output OSD_OUT with a video stream decoded by the video decoder 230, and outputs the resulting data to a video encoder 290. In this manner, the resulting data is displayed on a conventional television set, such that the conventional television set can perform a closed caption function.

The Takeuchi patent discloses a computer system that displays closed caption data on a display monitor of a computer (see Takeuchi, column 2, lines 29-33). In an example illustrated in Takeuchi, an MPEG decoder 203 comprises a RISC processor 601, a video decoder 603, an OSD circuit 605, and TEXT DATA 607 (see Takeuchi, Figure 16 and column 14, lines 19-21). The RISC processor 601 detects closed caption information in the form of text data from the input VIDEO STREAM (see Takeuchi, Figure 16 and column 14, lines 21-23). The TEXT DATA 607 is a bitmap file used for converting the closed caption text data received from the input VIDEO STREAM into bitmap data (see Takeuchi, Figure 16 and column 14 and lines 26-29). The OSD circuit 605 of Takeuchi receives the bitmap data from the RISC processor 601

and outputs the processed information to a synthesizing circuit 602 (see Takeuchi, Figure 16 and column 14, line 31-35). The synthesizing circuit 602 synthesizes the processed information with video data supplied from the decoder 603 and outputs the synthesized data to an MPEG image memory 503. The MPEG image memory 503 supplies the synthesized data to a video port controller 502, which in turn outputs the synthesized data to a VGA controller 113 (see Takeuchi, column 14, lines 58-67).

It is submitted that Takeuchi fails to teach or suggest the present invention as claimed in claim 1. In particular, it is submitted that Takeuchi fails to teach or suggest a "text OSD module for receiving the OSD object data from the buffer interface unit as text OSD data and for transforming the text OSD data and outputting text pixel data" and a "bitmap OSD module for receiving the OSD object data from the buffer interface unit as bitmap OSD data and for transforming the bitmap OSD data and outputting bitmap pixel data," as claimed in claim 1. Instead, Takeuchi discloses that the RISC processor 601 of Takeuchi receives text data and converts the closed caption data (in the form of text data) into bitmap data. There is no disclosure in Takeuchi of a "text OSD module" or a "bitmap OSD module." Moreover, since Takeuchi performs a single conversion of text to bitmap data, it follows that Takeuchi fails to teach or suggest "OSD object data" being received as "text OSD data" by the "text OSD module" and being received as "bitmap OSD data" by the "bitmap OSD module," as claimed in claim 1. Thus, it follows that Takeuchi fails to teach or suggest the "text OSD module... for transforming the text OSD data and outputting text pixel data" or a "bitmap OSD module...for transforming the bitmap OSD data and outputting bitmap pixel data," as claimed in claim 1.

In addition, since Takeuchi fails to teach or suggest the "text OSD module...for outputting text pixel data" and the "bitmap OSD module...for outputting bitmap pixel data," it therefore follows that Takeuchi fails to teach or suggest "an OSD mixer for receiving the text pixel data and the bitmap pixel data and outputting the resulting mixture as the pixel data output," as claimed in claim 1.

With regard to claim 4, it is submitted that Takeuchi likewise fails to teach or suggest "generating text OSD data and bitmap OSD data from the OSD object data," as claimed in claim 4, for reasons similar to those described above.

In addition, with regard to claim 4, Takeuchi fails to teach or suggest "transforming at least one of the text OSD data and bitmap OSD data into text pixel data and bitmap pixel data, respectively, if the OSD Enable signal has been generated," as claimed in claim 4, for reasons similar to those described above.

In addition, with regard to claim 4, Takeuchi fails to teach or suggest "mixing the text pixel data and the bitmap pixel data to produce a pixel data output," as claimed in claim 4, for reasons similar to those described above.

For these reasons, it is submitted that Takeuchi fails to teach or suggest these specific elements of the invention set forth in the amended claims. Reconsideration of the rejections of claims 1 and 4 under 35 U.S.C. 102(e) based on Takeuchi is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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